

# MN3005

## 4096-STAGE LONG DELAY BBD

### General description

The MN3005 is a world's first 4096-stage long delay BBD, 8 times longer than 512-stage BBD manufactured by using a P-channel low noise silicon gate process.

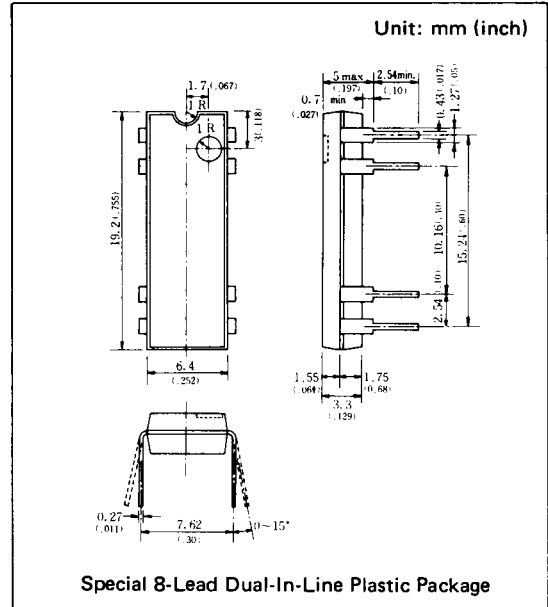
Long signal delay time 205ms can be obtained at clock frequency 10KHz. S/N is 75dB. S/N has been improved by more than 20dB in comparing with 8-connected 512-stage BBD's. The MN3005 is suitably used for reverberation and echo effects in electronic musical instruments such as electronic organ, guitar amplifier and music synthesizer which need long delay time.

### Features

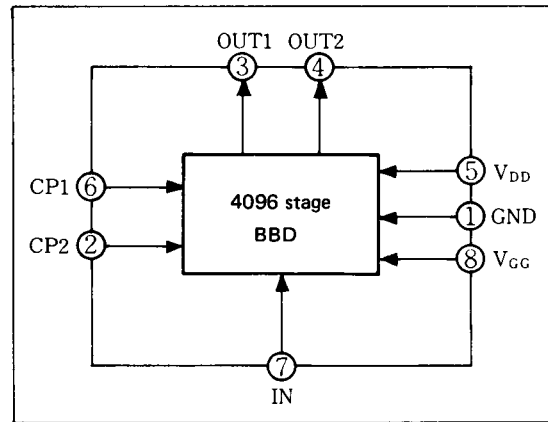
- 1 chip 4096 stage and wide range of variable delay times: 20.48 ~ 204.8ms.
- High S/N in spite of multi-stage and wide dynamic range: S/N  $\approx$  75dB typ.
- No insertion loss since the loss occurring in the signal transfer is corrected by the MOS capacity of input and output.  $L_i = 0$ dB.
- High integration and high reliability by using P channel low noise silicon gate process.
- Special 8 lead dual-in-line plastic package.

### Applications

- Reverberation and echo effects in echo microphone and stereo equipment.
- Chorus effect in electronic musical instruments.
- Variable or fixed delay of analog signals.
- Telephone time compression and delay line for voice communication systems, etc.



### Block Diagram



### Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	$V_{DD}, V_{GG}$	-15, $V_{DD} + 1$	V
Signal Delay Time	$t_D$	20.48~204.8	ms
Total Harmonic Distortion	THD	1	%
Signal to Noise Ratio	S/N	75	dB

■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V <sub>DD</sub> , V <sub>GG</sub> , V <sub>CP</sub> , V <sub>I</sub>	-18~+0.3	V
Output Voltage	V <sub>O</sub>	-18~+0.3	V
Operating Temperature	T <sub>opr</sub>	-20~+60	°C
Storage Temperature	T <sub>stg</sub>	-55~+125	°C

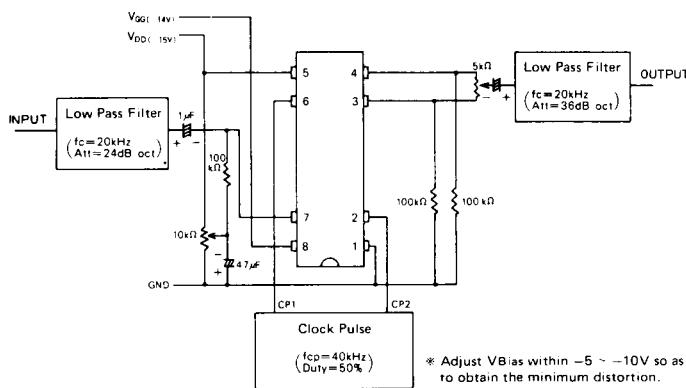
■ Operating Conditions (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V <sub>DD</sub>		-14	-15	-16	V
Gate Supply Voltage	V <sub>GG</sub>			V <sub>DD</sub> + 1		V
Clock Voltage "H" Level	V <sub>CPH</sub>		0		-1	V
Clock Voltage "L" Level	V <sub>CPL</sub>			V <sub>DD</sub>		V
Clock Input Capacitance	C <sub>CP</sub>				2800	pF
Clock Frequency	f <sub>CP</sub>		10		100	kHz
Clock Pulse Width *2	t <sub>cpw</sub>	Test Circuit			0.5T*2	
Clock Rise Time *2	t <sub>cpr</sub>	Test Circuit			500	ns
Clock Fall Time *2	t <sub>cpf</sub>	Test Circuit			500	ns
Clock Cross Point	V <sub>x</sub>		0		-3	V
Input DC Bias Voltage	V <sub>Bias</sub>		-5		-10	V

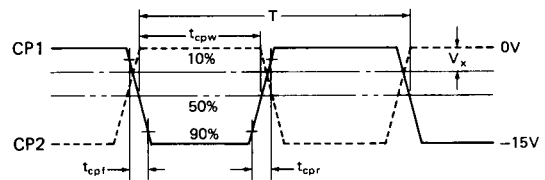
■ Electrical Characteristics (Ta = 25°C, V<sub>DD</sub> = V<sub>CPL</sub> = -15V, V<sub>CPH</sub> = 0V, V<sub>GG</sub> = -14V, R<sub>L</sub> = 100kΩ)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t <sub>D</sub>		20.48		204.8	ms
Input Signal Frequency	f <sub>i</sub>	f <sub>cp</sub> = 40kHz, V <sub>i</sub> = 1.0Vrms, Output Attenuation ≤ 3dB (0dB at f <sub>i</sub> = 1kHz)	10			kHz
Input Signal Swing	V <sub>i</sub>	f <sub>cp</sub> = 40kHz, f <sub>i</sub> = 1 kHz, THD = 2.5%	1.0			Vrms
Insertion Loss	L <sub>i</sub>	f <sub>cp</sub> = 40kHz, f <sub>i</sub> = 1 kHz, V <sub>i</sub> = 1.0Vrms	-4	0	4	dB
Total Harmonic Distortion	THD	f <sub>cp</sub> = 40kHz, f <sub>i</sub> = 1 kHz, V <sub>i</sub> = 0.78Vrms		1	2.5	%
Noise Voltage	V <sub>no</sub>	f <sub>cp</sub> = 100kHz Weighted by "A" curve			0.4	mVrms
Signal to Noise Ratio	S/N			75		dB

■ Test Circuit

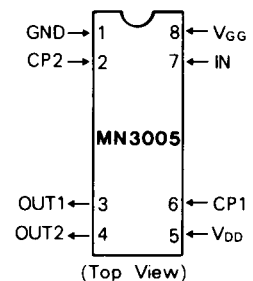


\* 1 Clock Pulse Waveforms

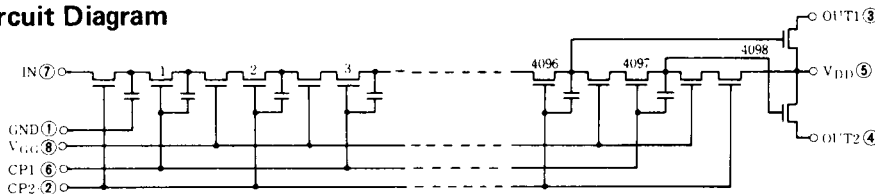


\* 2 T = 1/fcp

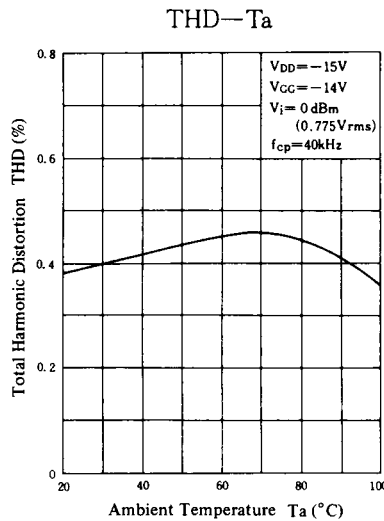
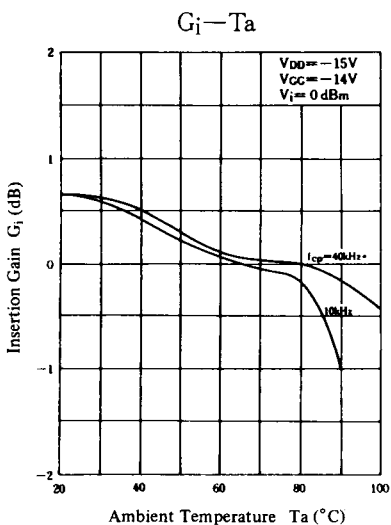
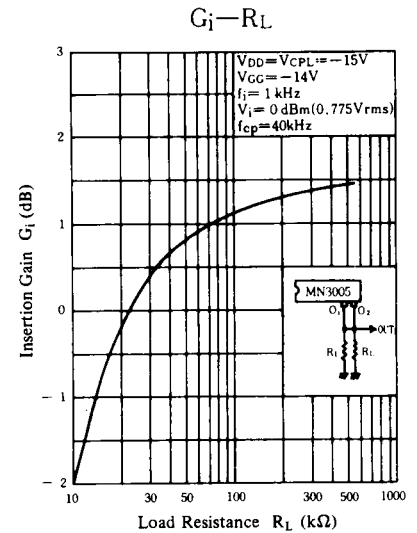
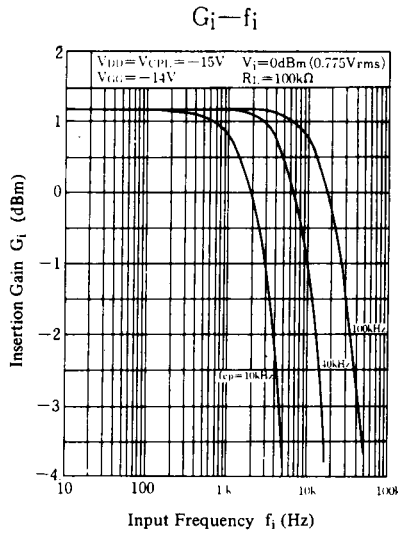
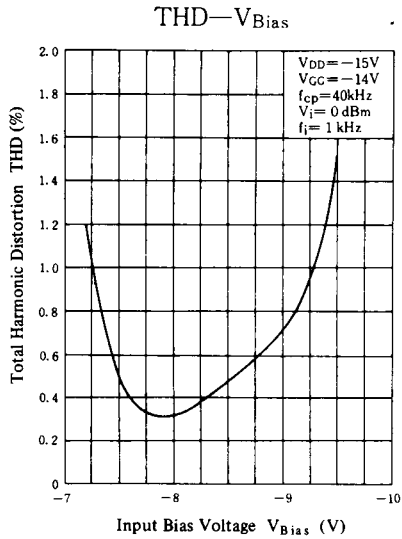
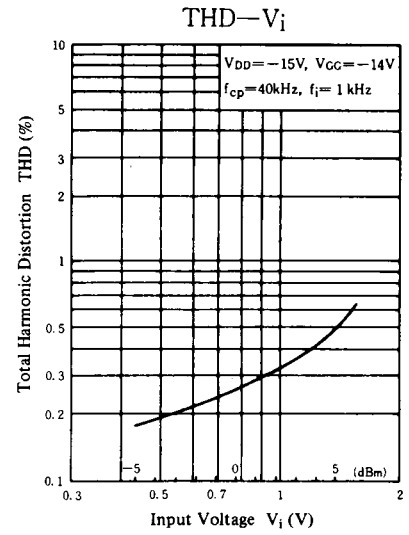
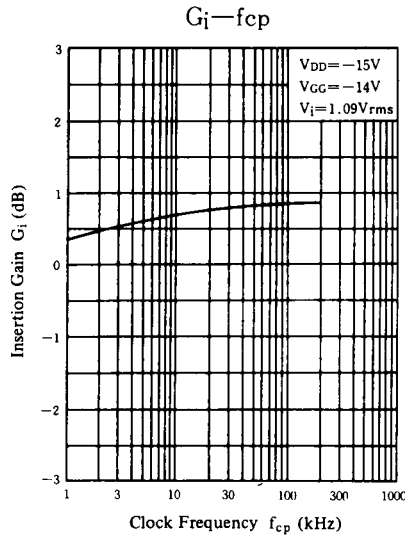
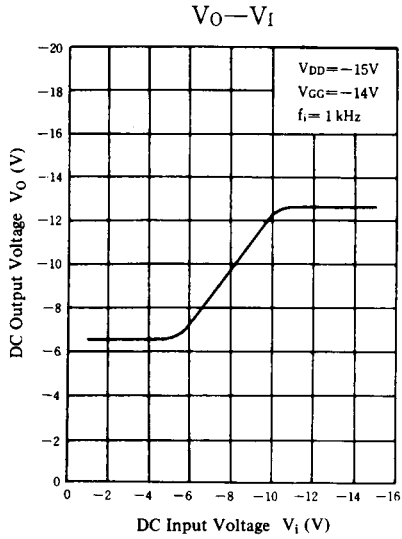
■ Terminal Assignments



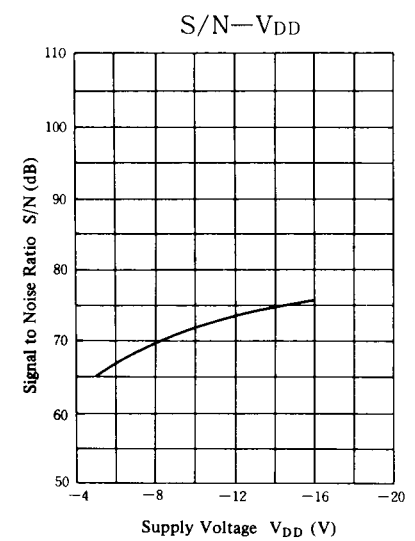
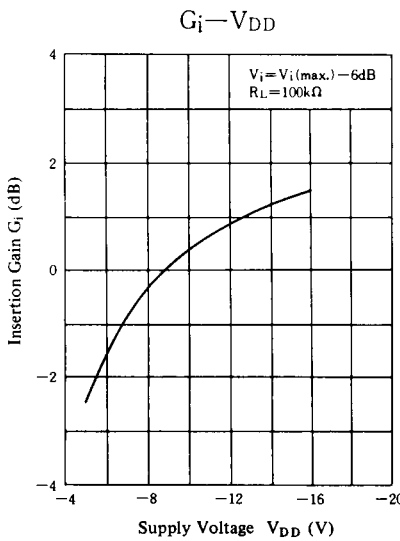
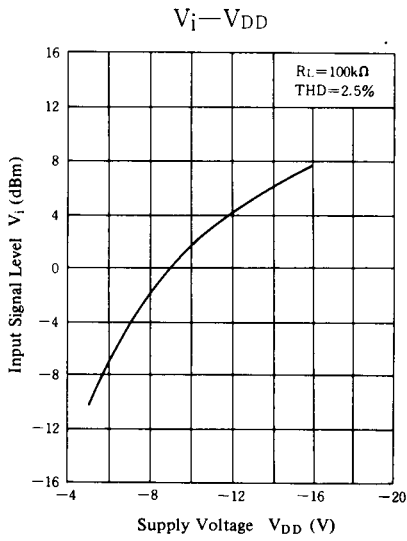
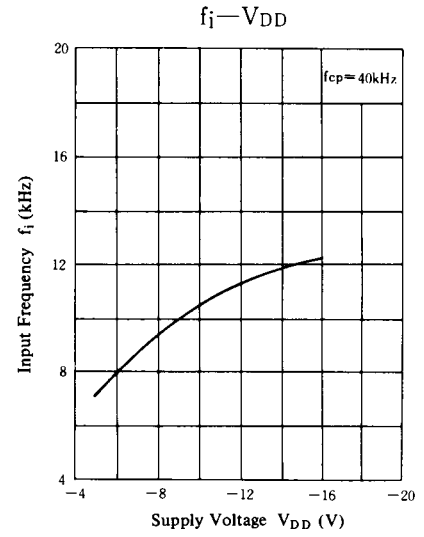
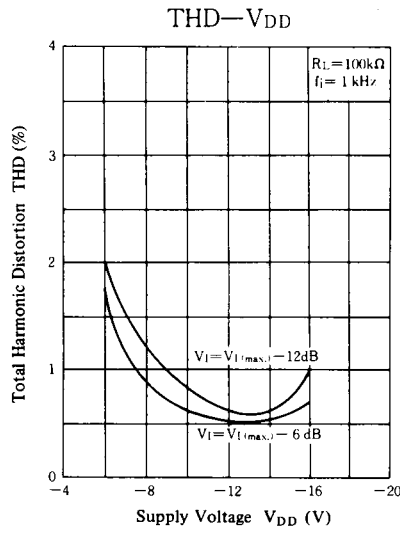
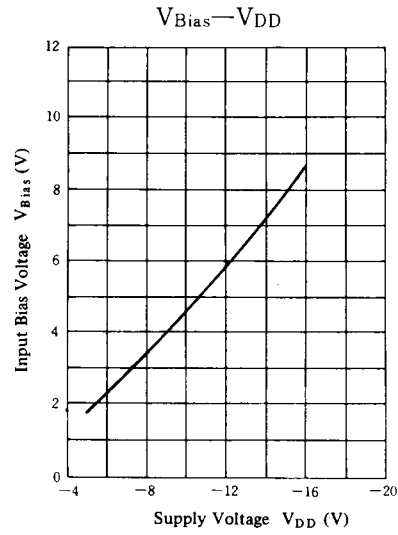
■ Circuit Diagram



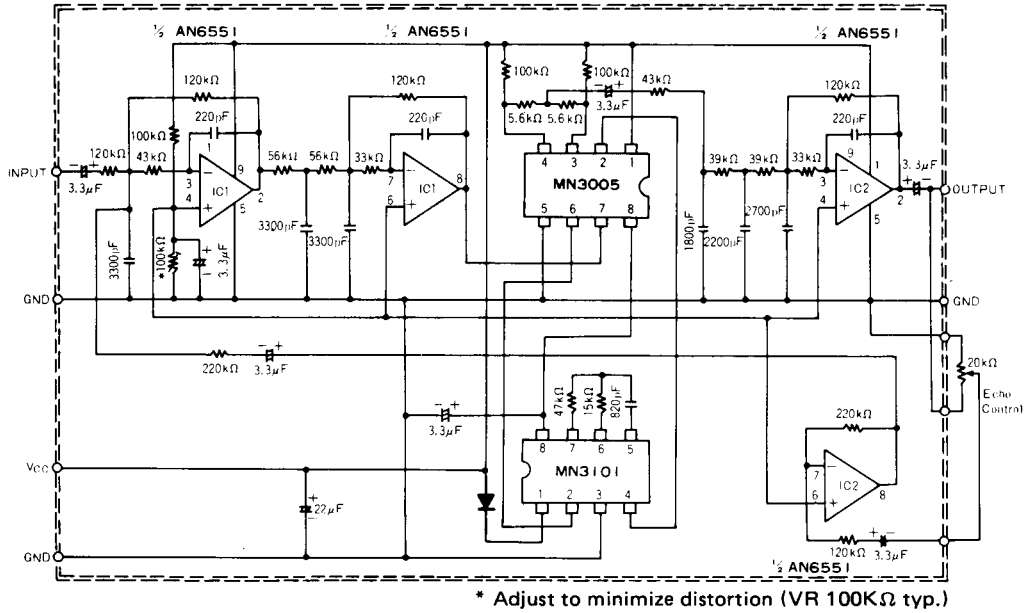
Typical Electrical Characteristic Curves



Supply Voltage Characteristics



■ Application Circuit



Reverberation Effect Generation Circuit (Signal Delay Over 100msec.)

■ Pattern Drawing of the Printed Circuit Board (Real size)

